RELAXATION OSCILLATOR CIRCUIT DESIGN FOR IMAGE SEGMENTATION

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Abstract: *This work presents a relaxation oscillator circuit design, which can be used as a part of an oscillator network applied for image segmentation. The hardware realisation of such a network can provide much faster image segmentation compared to computer simulation techniques. The segmentation method based on oscillator network was briefly described. New mathematical and circuit oscillator models were proposed along with simulation results. Also, the segmentation of sample binary image was presented, using the proposed mathematical oscillator model.*

1. Introduction

Segmentation of images into disjoint homogeneous regions is a very important aspect of visual perception. Although this process is relatively easy to be performed by humans, the image segmentation problem remains unsolved in many image analysis tasks.

One of the recently developed tools used for texture segmentation is a network of synchronised oscillators [1, 6]. Network operation is based on "temporary correlation" theory [6], which attempts to explain scene recognition as performed by a human brain. This theory assumes that different groups of neural cells code different properties of homogeneous image regions (e.g. shape, texture). Monitoring of temporal activity of cell groups allows for scene segmentation. To implement this theory, Wang [6] proposed an oscillator model to emulate neural cell and oscillator network for image segmentation.

Network dimensions are equal to dimensions of an analysed image and each oscillator represents a single image pixel (Fig. 1). The oscillators are connected to each other using positive synaptic weights (W_{ik} in Fig. 1). Their values are equal to 1 if two connected oscillators represent an image object and 0 otherwise. Due to these local excitatory connections, an active oscillator spreads its activity over the whole oscillators group, which represents image object. This provides synchronisation of the whole group. This synchronisation process is sequentially repeated for other oscillator groups, which represent different objects. The role of the global inhibitor (GI in Fig. 1) is to provide desynchronisation of oscillators groups representing objects different from the one which is actually being under synchronisation. The most detailed description of the oscillator network can be found in [1, 6].

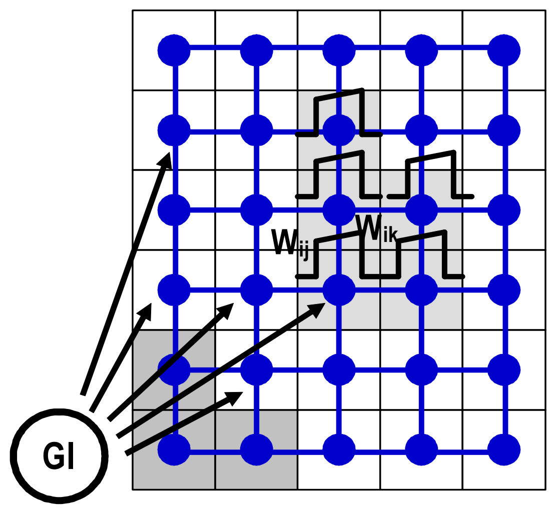


Fig. 1. Sample oscillator network.

It was demonstrated, that this network was successfully used for segmentation of Brodatz [1] and biomedical textures [5].

Hardware realisation of this network will speed up image segmentation. The structure of the oscillators' network suits very well for such implementation. They will be synchronised in parallel, leading to much faster image analysis than computer simulation.

Such a network was realised as integrated circuit [2] in AMS 0.8μm CMOS technology. The oscillator circuit in [2] was designed empirically without previous mathematical modelling. This paper presents a new mathematical oscillator model. It is more flexible than proposed in [2], allowing for a better control of network synchronisation and desynchronisation. Also, the new circuit oscillator model along with its simulations is described. This circuit has been designed using CADENCE version 4.4.6 04/03/2002 in AMIS 0.35µm C035M-D 5M/1P technology. The oscillator circuit can be further used for the whole network structure design. Computer simulations of the network using the proposed mathematical oscillator model are also presented.

2. A new mathematical oscillator model

In the network proposed in [1, 6] oscillators are described by two differential equations:

$$\frac{dx}{dt} = 3x - x^3 + 2 - y + I_{inp} \tag{1}$$

$$\frac{dy}{dt} = \varepsilon\left[\gamma\left(1 + \tanh\left(\frac{x}{\beta}\right)\right) - y\right] \tag{2}$$

where x is referred to as an excitatory variable while y is an inhibitory variable. I_{inp} is a total external stimulation of an oscillator (in the simplest case it depends on pixel grey level) and ε, γ, β are parameters.

The following mathematical oscillator model, which can be physically realised using Operational Transconductance Amplifiers (OTA) is proposed:

$$C_1\frac{dV_1}{dt} = I_1\tanh(aV_1) - I_2\tanh(bV_1) - I_3\tanh(cV_2) + I_{inp} \tag{3}$$

$$C_2\frac{dV_2}{dt} = I_4\tanh(dV_1) - I_3\tanh(cV_2) \tag{4}$$

where V_1 is an excitatory variable while V_2 is an inhibitory variable. I_1, I_2, I_3, I_4, C_1, C_2 and a, b, c, d are constants. I_{inp} depends on the grey level value of the pixel connected to the given oscillator. A circuit representation of the oscillator model described by the above system of nonlinear differential equations (3) and (4) is shown in Fig. 2.

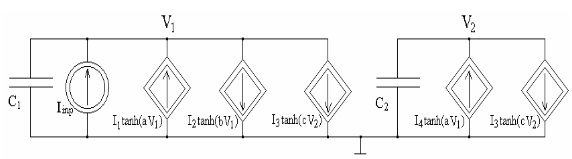


Fig. 2. A circuit representation of oscillator mathematical model.

The oscillation amplitude of the state variable V_1 can be expressed by the following equation:

$$A_{V1} = -\frac{1}{b}\,arc\tanh\left[\tanh\left(\sqrt{2}\frac{b}{a}\right) - \frac{2I_1}{I_2}\right] \tag{5}$$

Assuming A_{V1}=0.5V and taking into account the voltage and current limitations of the AMIS 0.35µm technology, the following oscillator parameter values were selected: I_1=1.2µA, I_2=2µA, I_3=2µA, I_4=2µA, a=10, b=2.44, c=2.44, d=500, C_1=15fF, and C_2=1.1pF.

Using the analytical short-channel Sakurai-Newton MOSFET model [4] with parameter LAMBDA=0 and neglecting body effect, the following expression determines the $I_o(V_r)$ transfer characteristic of the OTA [3]:

$$I_o = \begin{cases} I_{sat} & for \quad V_r \geq \sigma \\ -I_{sat} & for \quad V_r \leq -\sigma \end{cases}$$

$$V_r = \sqrt[n_r]{\frac{(I_{sat} + I_0)L_{EFFr}}{2W_rB_r}} - \sqrt[n_r]{\frac{(I_{sat} - I_0)L_{EFFr}}{2W_rB_r}} \quad for \ -\sigma < V_r < \sigma \tag{6}$$

where V_r is the differential input voltage of the OTA, B_r – differential pair MOSFETs saturation current factor, W_r and L_{EFFr} – width and effective length of differential pair MOSFETs respectively, n_r – saturation current coefficient of differential pair transistors, I_{sat} and σ – saturation current and saturation voltage of OTA respectively. The transfer characteristic described by equation (6) can be approximated by the following expression:

$$I_o = I_{sat}\tanh\left(n_r \cdot 2^{\frac{1-n_r}{n_r}}\sqrt[n_r]{\frac{B_rW_r}{I_{sat}L_{EFFr}}} \cdot V_r\right) \tag{7}$$

An example of the approximation of function (6) by means of function (7) is shown in Fig. 3.

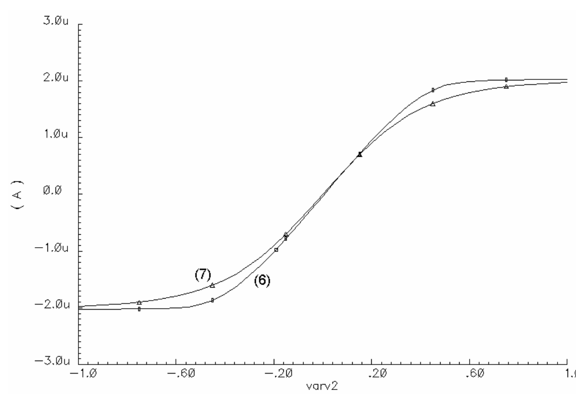
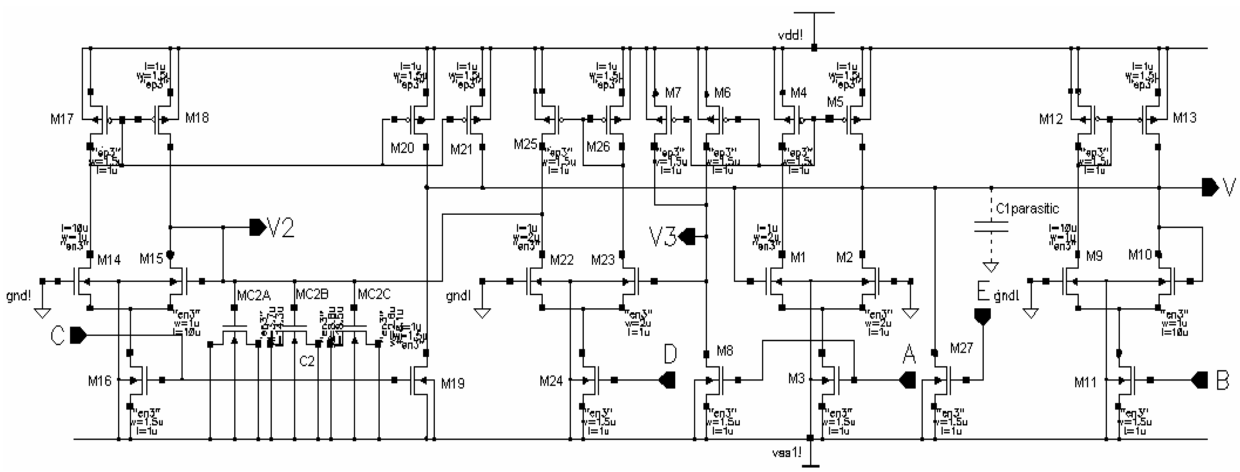


Fig. 3. Approximation of function (6) by means of function (7).

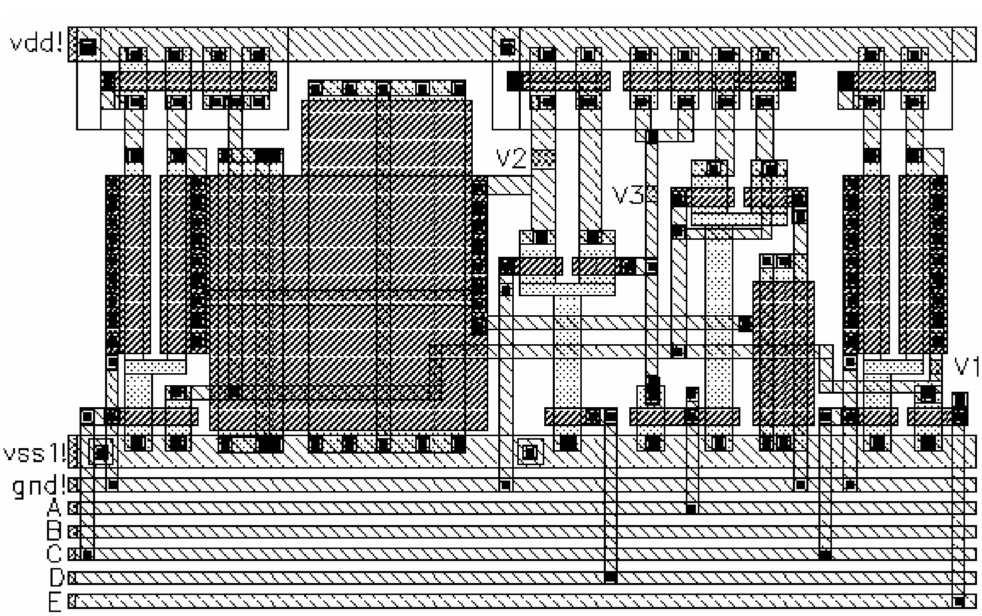
3. Oscillator CMOS circuit

Using circuit representation of oscillator mathematical model presented in Fig. 2 its CMOS circuit OTA-based structure has been designed. Scheme of the oscillator CMOS circuit is presented in Fig. 4a. Transistors M1-M5 realise the function $I_1\tanh(aV_1)$, transistors M9-M13 realise the function $I_2\tanh(bV_1)$, M14-M21 realise two functions $I_3\tanh(cV_2)$, transistors M6-M8 and M22-M26 realise the function

$I_4 \tanh(dV_1)$, while transistor M27 plays the role of current source I_{inp}. Transistor dimensions have been designed to ensure that all MOS transistors always work in saturation region for assumed oscillations amplitude. Layout of the oscillator circuit shown in Fig. 4b has been designed using CADENCE. In order to save silicon area capacitor C_2 has been implemented using the gate capacitances of the three transistors MC2A, MC2B and MC2C. Because the channels of these transistors are working in strong inversion continuously, equivalent capacitance of such structure is linear for the assumed oscillations amplitude of both state variables V_1 and V_2. Capacitor C_1 is implemented by a sum of parasitic layout capacitances – $C1_{parasitic}$ (Fig. 4a). Oscillator layout occupies 51μm × 32.5μm (1657μm^2) silicon area. With typical supply voltage 3.3V the supply current is about 12μA, so a power consumption by the oscillator is about 40μW.



(a)



(b)

Fig. 4. Schematic (a) and layout (b) of the oscillator circuit.

The oscillator CMOS circuit has been simulated using connection to biasing circuits as shown in Fig. 5. Spectre transient simulation results of oscillator voltage waveforms V_1, V_2, V_3 are shown in Fig. 6. The voltage waveform V_3 is a binarised voltage V1 with the threshold equal to zero. The simulation has been performed using BSIM3v3.2 Level 53 MOS transistor model taking all layout parasitic capacitances into consideration.

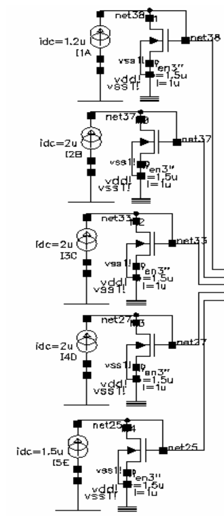


Fig. 5. The connection of the oscillator circuit to biasing circuits.

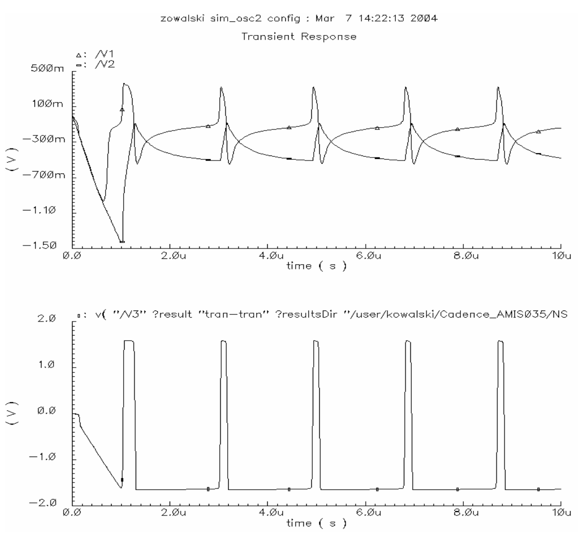


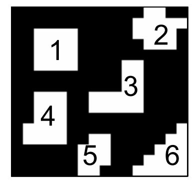
Fig. 6. Simulated waveforms of oscillator voltages $V_1(t)$, $V_2(t)$, $V_3(t)$ for I_{inp}=-1.5μA.

4. Software simulation of the oscillator network

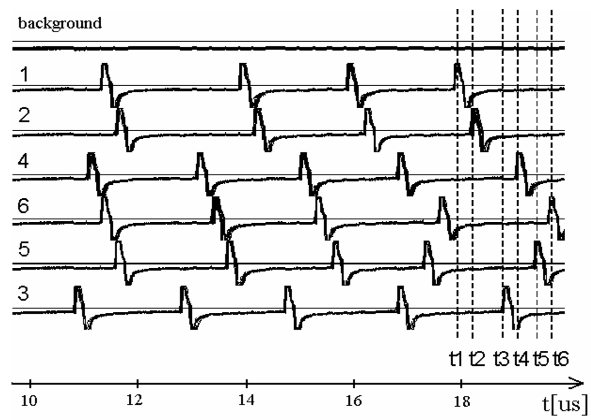
To analyse the oscillator model described by eq. (3), (4) a matrix network with 16×16 oscillators was simulated using Borland Delphi software. The total external excitation of each oscillator *i* is defined by formula (8):

$$I^i_{inp} = I^i + \sum_{j=1}^{4} W_{ij} Hev(V_{1j}) - W_z z \qquad Hev(V) = \begin{cases} 0 & V < 0 \\ 1 & V \geq 0 \end{cases} \tag{8}$$

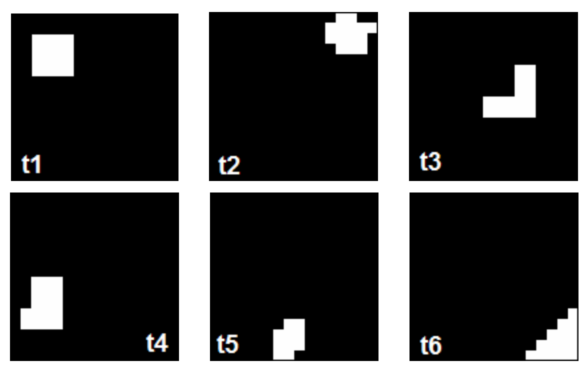
where I^i is the grey level of the image point connected to oscillator *i*, W_{ij} are weight values between this oscillator and its four neighbours, *z* is a global inhibitor (GI) variable. It is equal to one if at least one network oscillator is active, i.e. its output $V_1(t)$>0, otherwise *z* is equal to zero. W_z is a constant weight connected to GI. The GI ensures, that only one oscillator group (representing a given image object) is activated at the same time. A proper selection of W_{ij} and W_z values enables to control the network oscillators and provides their appropriate synchronisation and desynchronisation. Segmentation results of a sample binary image with 6 objects using simulated network are shown in Fig. 7.



(a)



(b)



(c)

Fig. 7. Sample binary image with 6 objects (a). Oscillator waveforms for oscillator groups connected to different image objects (b). Oscillator's activity maps (active oscillators marked in white) observed in time instants t1, t2, t3, t4, t5 and t6 (c).

Fig. 7b presents waveforms of oscillator groups connected to given image objects and background. It can be observed, that oscillators within a group are synchronised, whereas after some time different groups oscillate with faze shift. For selected time instants t1, t2, t3, t4, t5 and t6 it is possible to detect six image objects based on observed oscillator activity maps. These maps ensure correct image segmentation, as shown in Fig. 7c. Background oscillators are never activated, because grey level values of their connected points and weights W_{ij} are equal to zero, resulting in consequence $I^i_{inp} = 0$.

5. Conclusions

It was demonstrated, that the presented oscillator circuit model can be used for construction of an oscillator network able to perform segmentation of binary mages. The next step will be a design of synaptic weights and global inhibitor circuits. Then, a simulation of the whole network for sample binary images will be performed. An important problem is the maximum number of objects which can be detected by the network. In currently performed simulations it is equal to 6 and depends on the filling factor of oscillator period. However, the proposed flexible oscillator model allows for changing this factor if necessary, for example by increasing the current I_4. Another problem is to provide a gating mechanism, which allows for selection of time period, when all image objects will be recognised (all oscillator groups will be activated). This can be solved by applying an extra oscillator, not connected to the network, but to the global inhibitor only. If properly driven, it will periodically oscillate along with other oscillator groups. Analysis of network activity maps between this additional oscillations will ensure a detection of all image objects. These problems are topics of further research.

Acknowledgements

This work is supported by the Polish Ministry of Scientific Research and Information Technology under grant No. 4-T11B-041-25. Cadence support is provided by Imec and Europractice.

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