CMOS VLSI CHIP FOR SEGMENTATION OF BINARY IMAGES

Jacek Kowalski, Michał Strzelecki

Institute of Electronics, Technical University of Lodz, Wolczanska 223, 90-924 Lodz, Poland, emails: [jackowal,mstrzel]@p.lodz.pl

Abstract: *This paper presents a CMOS VLSI ASIC integrated circuit which implements a network of synchronised oscillators. This circuit was designed for segmentation of binary images, which is an important issue in biomedical image analysis. The hardware realisation of oscillator network provides much faster image segmentation compared to computer simulation techniques. The network chip architecture was briefly described and functional tests of selected circuit blocks were presented. Also, segmentation results of sample binary image obtained using oscillator network chip were discussed.*

1. Introduction

Segmentation and labelling of binary images is a very important aspect of biomedical image analysis. For example, in dermatology skin mast cell microscopic images are analyzed in order to calculate their number and area in comparison to the whole cell. To calculate these parameters, mast cells were segmented from the image background. Mast cells' area and its number suggest role importance of those structures in activation of mast cells and points out at the role of mast cell themselves in both physiological and pathological processes in the organism [5].

Among a large variability of image segmentation tools, a network of synchronised oscillators [1, 6] is very promising method. Its operation is based on "temporary correlation" theory [6], which attempts to explain scene recognition as performed by a human brain. This theory assumes that different groups of neural cells code different properties of homogeneous image regions (e.g. shape, texture). Monitoring of temporal activity of cell groups allows for scene segmentation. To implement this theory, Wang [6] proposed an oscillator model to emulate neural cell and oscillator network for image segmentation. It was demonstrated, that this network was successfully used for segmentation of Brodatz [1] and biomedical textures. Detailed description of network operation can be found in [6].

This network is suitable for hardware realisation. This will speed up image segmentation. The structure of the oscillators' network suits very well for such implementation. The mathematical oscillator model for hardware realisation was proposed in [2,3]. Also, some network functional blocks were described in [4] along with their Spectre simulations results.

This paper presents a VLSI ASIC CMOS integrated circuit, which implements the oscillator network architecture. The chip block diagram is discussed and functional tests of selected network blocks are presented. Also, preliminary image segmentation results obtained using the network chip are described. The circuit was realised in AMIS 0.35µm C035M-D 5M/1P technology by Europractice, and it contains a matrix with 8x8 size.

2. The network chip architecture

In this section, a concept of image segmentation processor with structure of synchronised oscillator's network has been presented. It was taken into consideration that characteristics of oscillators are described by continuous analytical functions and the best way of realisation technique will be analogue one. It was assumed that the processor will co-operate with IBM PC computer or workstation. Because computer busses are using digital signals, input/output circuits of the processor should be realised in digital technology. That is why it was considered that the processor will be realised as ASIC (Application Specific Integrated Circuit). In this case it is possible to combine analogue technology with digital one in a single chip.

A block diagram of processor of synchronised oscillator's network is presented in Fig. 1.

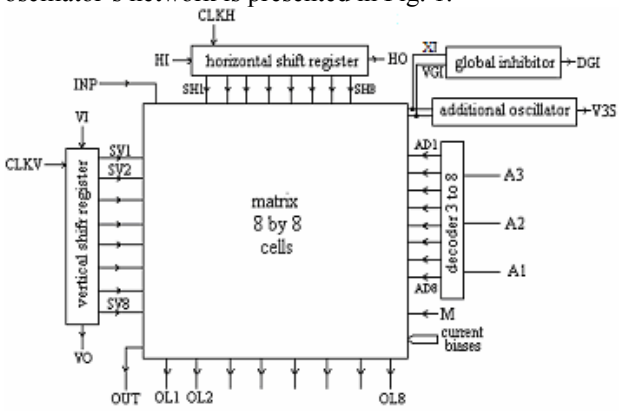


Fig. 1. A block diagram of synchronised oscillator's network processor.

The main element of the chip is a matrix 8 by 8 cells, which are processing units of image pixels. Each cell consists of oscillator CMOS circuit, excitatory synapse (network weights), input and output circuits. An image is fed into network chip by serial input INP, pixel by pixel and line by line. Cells are addressed by two shift registers: horizontal and vertical. Shift registers are controlled by two clocks: CLKH and CLKV. Signals HI and VI are used to synchronise image loading. Control signals required for writing the input image pixels into a chip are shown in Fig.2.

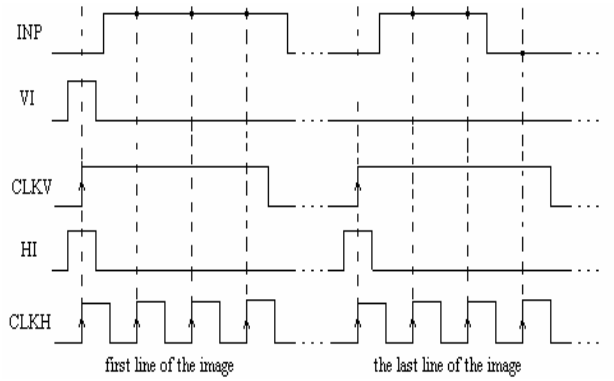


Fig.2. Control signals required for input image loading into a chip.

Global inhibitor circuit (GI) is connected to all oscillators in the network. This circuit uses two signals: VGI and XI. Node VGI is activated when at least one oscillator in the network is active. DGI output signal is a binarised version of VGI, it is used for observation of global inhibitor circuit state. Line XI is used for inhibit all oscillators, when GI is active. An additional oscillator, connected to the whole network by weights, is connected to GI only. This oscillator was implemented to synchronise operation of the oscillator network. It allows also for counting the number of recognised image objects. V3S is an output signal of this oscillator.

Segmented image objects can be outputted by a serial digital signal OUT. This output is controlled in the same way as input INP by horizontal and vertical registers. It is also possible to observe an activity of selected oscillator's row of the network. This row is addressed by a 3 to 8 decoder. Then, oscillator's states are available in digital outputs OL1-OL8. During network chip testing, a latter described parallel technique was used for observation and analysis of oscillator's outputs.

Thus a network chip is a mixed signal analogue-digital circuit. Global inhibitor and additional oscillator circuits are fully analogue, matrix of 8 by 8 cell containing oscillator and its additional circuits is analogue in the most part, while shift registers and line decoder are typically digital.

3. A test of basic chip building blocks

A basic building block of the chip is CMOS oscillator circuit. Schematic of the oscillator circuit is shown in Fig. 3.

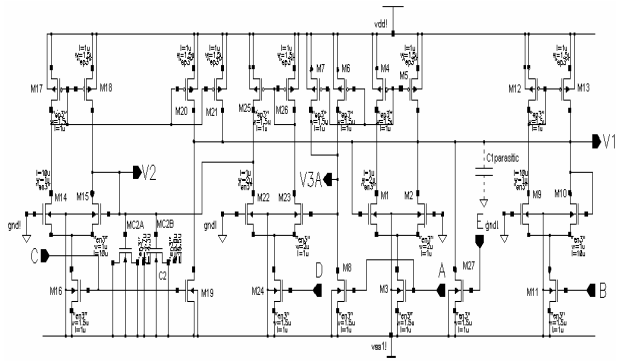


Fig. 3. Schematic of the oscillator circuit.

This CMOS oscillator has been described in [2,3,4] in details. The oscillator circuit has been implemented in the chip in form of a separate test structure. A schematic of oscillator test structure is presented in Fig.4.

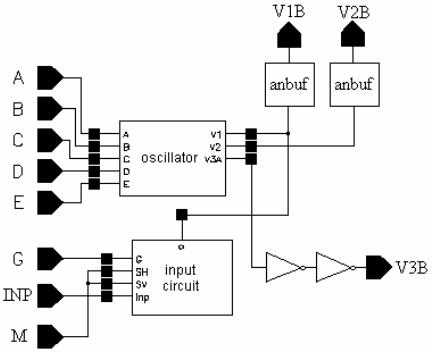


Fig. 4. Schematic of oscillator test structure.

The test structure is composed of the oscillator CMOS circuit, two analogue buffers, one digital buffer and input circuit. V1B is an excitatory variable of the oscillator, V2B is an inhibitory state variable and V3B is binarised voltage V1B with a threshold equal to zero. This test structure has been measured using a set-up shown in Fig. 5.

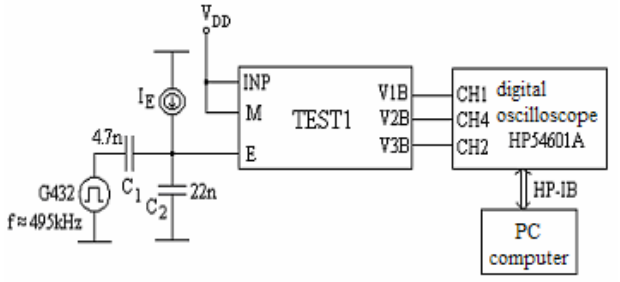


Fig. 5. Set-up for measurements of test structure implemented in the chip.

The set-up contains the measured test structure TEST1, digital oscilloscope coupled with PC computer using HP-IB interface and a generator for trials of extrinsic synchronisation of CMOS oscillator. Oscillograms of CMOS oscillator structure waveforms are shown in Fig. 6. These waveforms are correct and agree with computer simulations performed using Spectre software during chip design [3,4].

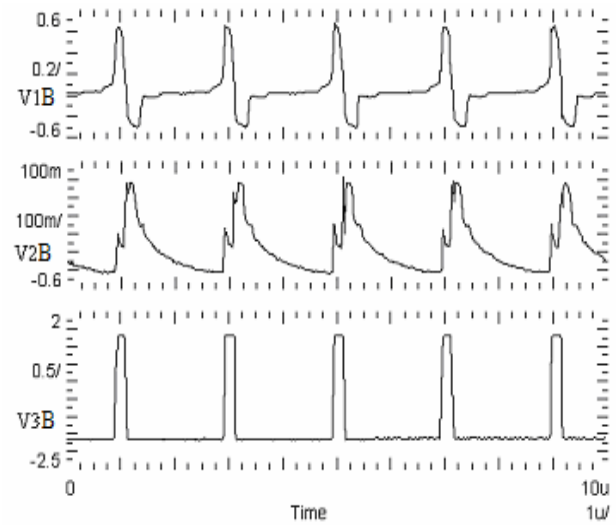


Fig. 6. Oscillograms of V1B, V2B, V3B waveforms of CMOS oscillator structure.

4. Segmentation results of sample binary images using network chip

In this section, a preliminary results of binary images segmentation using a network chip has been described. To perform image segmentation, an experimental laboratory bench was constructed. Its bloc diagram is shown in Fig. 7.

This bench consists of the following elements:

- PC computer,
- universal I/O PCI card NI PCI 7831R by National Instruments,
- special module containing an integrated circuit of oscillator network.

A PC computer working under MS Windows XP and LabView ver. 7.1 software was used to program the NI PCI 7831R card. This I/O card has 96 digital reconfigurable inputs/outputs, their operating frequency is 40 MHz. This card also contains an internal FPGA structure. 8 card connectors were configured as outputs. They were used to input a binary image to the network chip. There were: CLKH, SI, CLKV, SI and INP. Another 3 inputs were used for addressing one of 8 network rows for oscillator's output reading (signals A1, A2 and A3 in Fig. 1). Another 10 card connectors were configured as inputs. 8 of them (OL1,...,OL8 in Fig. 1) are used for getting the oscillators outputs of a given network row (addressed by A1-A3). Another two are used for reading the states of GI circuit (DGI) and an additional oscillator (V3S).

I/O card is connected to a special external test module which contains a chip with oscillator network. This module possess also I/O buffers (for input and output data and row address) and circuits designed for chip control. There are polarization currents used for setting of oscillator network weights, weight of GI circuit and to control other oscillator parameters (like its characteristics shape [2,3]). It is also possible to switch on/off an additional oscillator (AO) and global inhibitor (GI) circuits.

Software written in LabView allows to edit/store/read from a hard disk a sample binary image. Next, this image can be written to the network chip. Image pixels are serially transferred to the chip using synchronization signals SI and VI as described in section 2. Because of the charge leakage in CMOS structures, the image has to be loaded repeatedly. The refreshing time can be controlled by the LabView software. This software is stored inside of FPGA structure and allows refreshing period starting from 1 ms with a step equal to 1 ms.

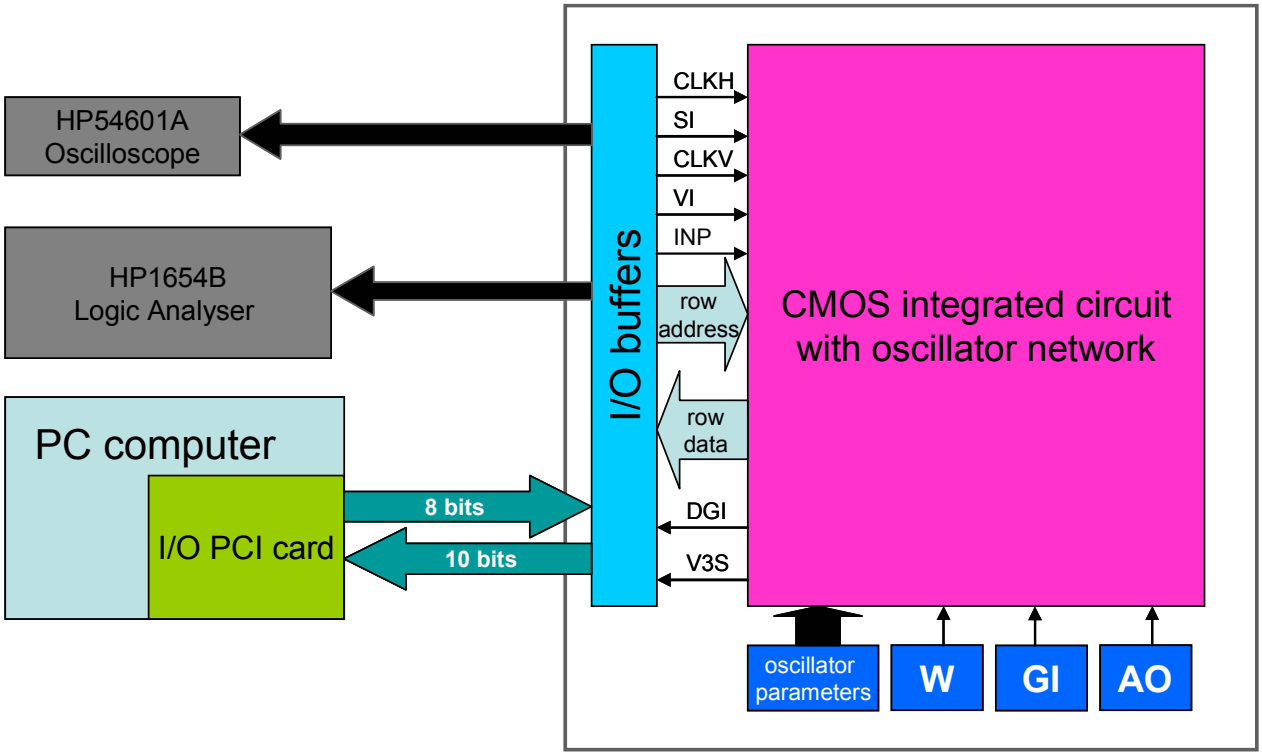
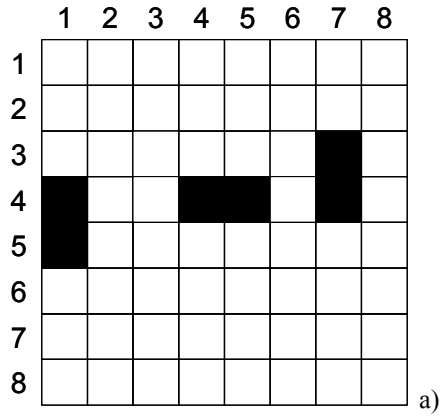
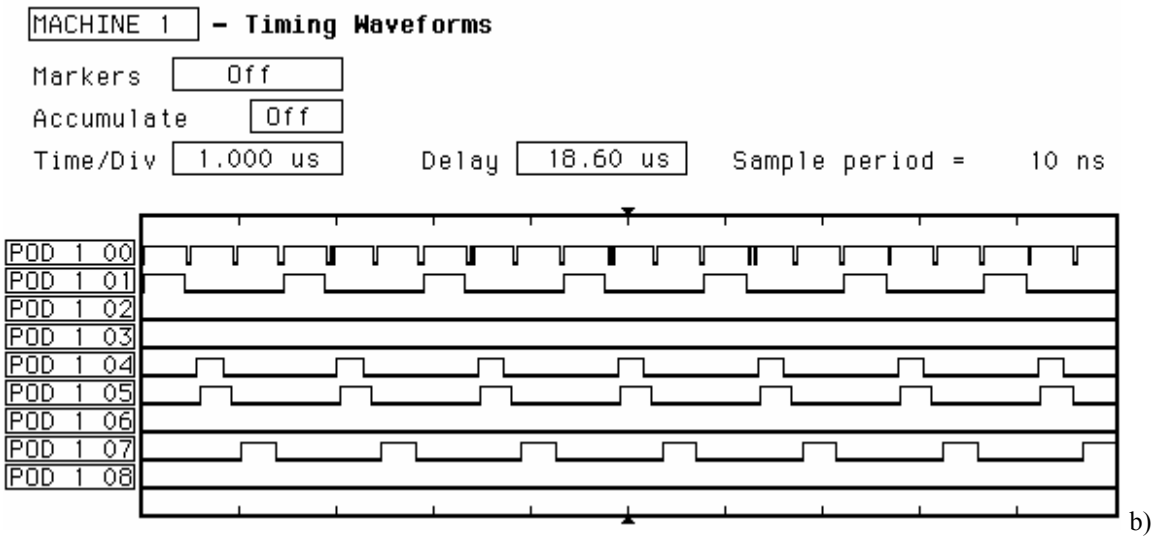


Fig. 7. The bloc diagram of experimental laboratory bench for binary image segmentation



a)



b)

Fig. 8. Sample binary image with 3 objects (a), output waveforms of oscillators (row 4, POD 1 00-08) and GI (POD 1 00) (b).

Measurements of chip parameters demonstrated, that refreshing time should be no shorter than 4-5 s. After image is loaded into the network, the oscillators start to oscillate. Oscillators output can be obtained for each row, which address is controlled by the software. Another row can be observed after address change performed by the I/O card. Appropriate setting of polarisation currents which control network weights and GI weight allow to find a stable network state, where oscillators connected to given image object are in synchrony, while oscillator groups representing different objects are desynchronized.

For observation of network state a digital oscilloscope HP54601A was used. It is connected to the PC computer using HP-IB interface, which allows for oscillograms storage. Also, for oscillator waveforms observation and storage, a logic analyser HP1654B was applied. Oscillator waveforms are also written to I/O card by LabView software, which allows for image segmentation based on waveform analysis.

Sample binary image used for network chip segmentation is shown in Fig. 8a. It contains three objects defined in such a way, that at least a part of each object is localised in row no. 4. This allows for observation of network behaviour in a given time (this is because simultaneous observation of oscillators outputs of one row is available only). The refreshing period was equal to 1s. After loading the image, the network tuning process was started to check whether it possible to get oscillator synchronisation for image objects. This process involved a change of network weights polarisation current. After such synchronisation was obtained, the global inhibitor circuit was turned on and regulation of polarisation current of GI network was performed. This was done to obtain a desynchronisation between oscillators belonging to different object groups. Oscillator waveforms obtained for line 4 are presented in Fig. 8b. It can be observed, that oscillators 4 and 5 are in synchrony, while oscillators 1, 4 and 5, 7 are desynchronised. As a consequence, waveform analysis of these oscillators (and also waveforms of oscillators 7 from row 3 and oscillator 1 from row 5, not shown in Fig. 8b) allows for segmentation of image shown in Fig. 8a. Segmentation time was 1 μs (one period of active oscillators). Fig. 8b contains also output waveform of GI. This waveform does not allow defining the end of image segmentation procedure. To do this, an additional oscillator (AO) should be turned on. Image segmentation using this oscillator is shown in Fig. 9. Fig. 9a presents a sample image with 2 objects, and Fig. 9b shows output waveforms of oscillators from row 4, and also waveforms of GI and the AO (denoted as POD 1 09 in

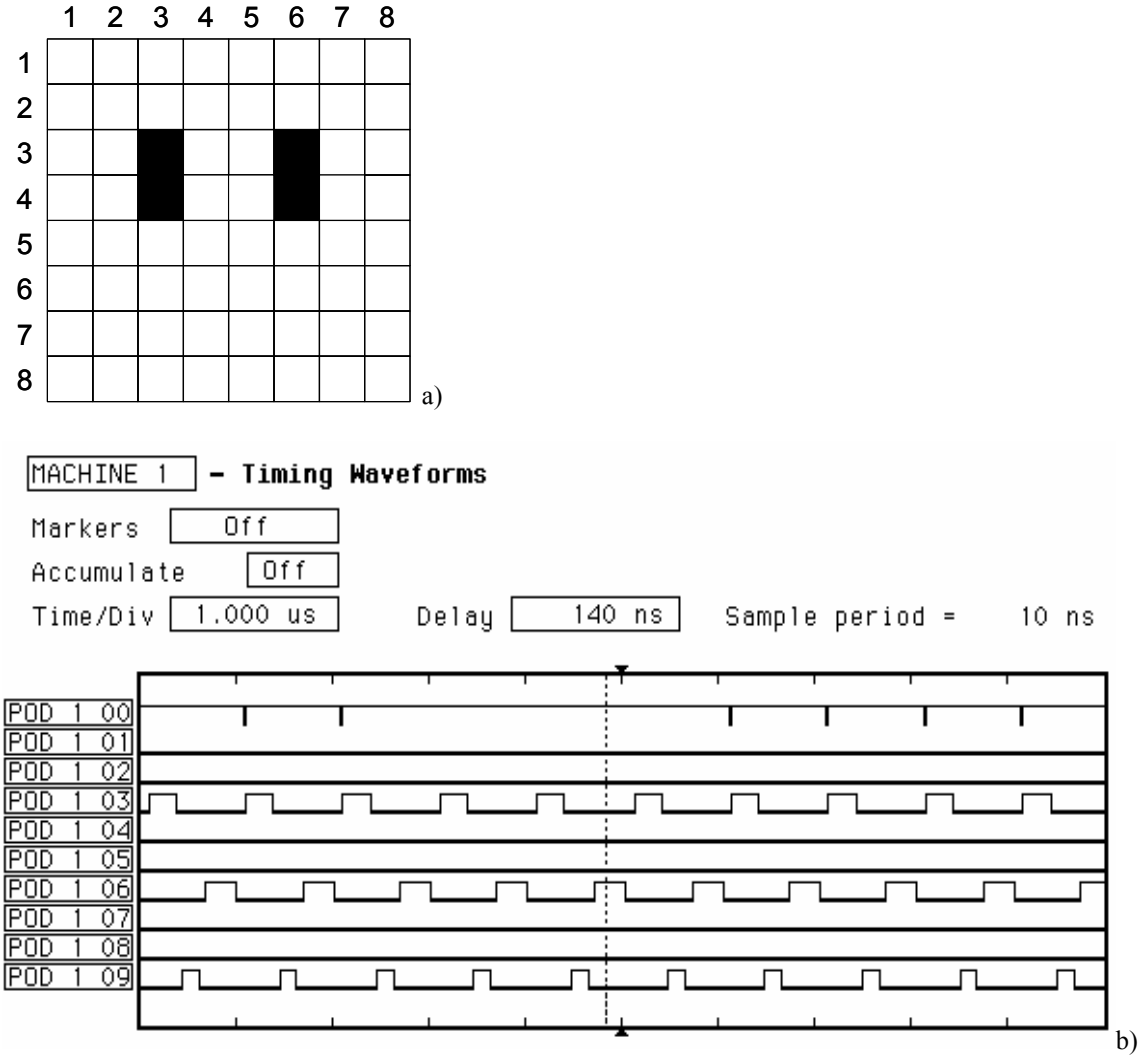


Fig. 9. . Sample binary image with 2 objects (a), output waveforms of oscillators (row 4, POD 1 00-08), GI (POD 1 00) and the additional oscillator (POD 1 09) (b).

Fig. 9b). Now, the image segmentation is performed between active states of the additional oscillator. Thus oscillator's waveform analysis could be limited to this period only. The additional oscillator can be considered as representing an „extra object", thus it is desynchronised with other oscillators groups (representing image objects). Because network oscillators oscillate continuously, an active state of this additional indicates the start of segmentation process and next active state tells, that image objects has been detected by the network and new segmentation network cycle has begun. Thus, information about objects detected by the network can be finding between AO active states. Segmentation time is this case was also equal to 1 μs.

5. Conclusions

Preliminary test results of integrated circuit implementing oscillators network shows, that this chip can be used for segmentation of binary images. It was demonstrated, that the new mathematical oscillator model [2,3] applied in the network oscillator circuit provides appropriate network operation (oscillators synchronization within an object and oscillators groups desynchronisation between different objects). Also, the idea of implementing an additional oscillator connected to global inhibitor only was successful. Analysis of output waveforms of this oscillator enables to find the start and stop time instants of image segmentation process (segmentation of whole image occurs between active states of this oscillator). Segmentation time of sample analysed images is equal to 1 μs, it does not depend on image size but on number of image objects only [6]. This time is much shorter if compared to computer simulations (several milliseconds for image of the same 8x8 size).

A one drawback of network chip observed during circuit testing was a limited number of objects in segmented image which can be recognised by the network (experiments demonstrated, that only 3 image objects can be segmented by the network chip so far). This is caused by different filling factors of oscillators output waveforms (this can be observed in Fig. 9b, where filling factors for oscillator 4 and 5 waveforms are different). Such differences influence desynchronisation process by increasing an resulting filling factor of oscillator group output waveform. An increment of this

filling factor leads to reduction of object number recognised by the network [6]. The filling factor variability of oscillators outputs is resulted by technological scatter of transistor parameters used for building of oscillator functional blocs. The influence of this phenomenon for oscillator characteristics was much higher than observed during Spectre software simulations of network chip. Further network circuit tests are planned comprising tuning of oscillator characteristics in order to reduce its output filling factor variability and in consequence to increment number of objects segmented by the network chip.

Acknowledgements

The authors wish to thank to Professor Alexis De Vos (University of Ghent, Belgium) for his help in the oscillator network chip designing in CMOS AMIS 0.35μm technology.

References

[1] Çesmeli E., Wang D., *Texture Segmentation Using Gaussian-Markov Random Fields and Neural Oscillator Networks*, IEEE Transactions on Neural Networks, **12**, 2, 2001, pp. 394-404.

[2] Kowalski J., Strzelecki M., De Vos A. *„Relaxation Oscillator Circuit Design for Image Segmentation*, Workshop Proceedings of IEEE Signal Processing'2004, pp.27 – 31, 24th September 2004, Poznań, Poland.

[3] Kowalski J., Strzelecki M., *"Measurement verification of functional blocks of VLSI CMOS integrated circuit of synchronised oscillators network for binary image segmentation",* IV Krajowa Konferencja Elektroniki – KKE'2005, Proceedings, Darłówko, Vol. 2/2, pp. 519 - 524, 12– 15.06.2005, Poland, (in Polish).

[4] Kowalski J., Strzelecki M., „*CMOS VLSI design of synchronised oscillators network for binary image segmentation"*, Proceedings of the 12th International Conference on Mixed Design of Integrated Circuits and Systems – MIXDES'2005, Kraków, Poland, pp. 71 - 76, June 22–25, 2005.

[5] Strzelecki M., Liberski P., Zalewska A., *Segmentation of Mast Cell Images Using network of Synchronised Oscillators*, Proc. of the International Conference Informatics for Health Care, Visaginas, 19-20 September 2002, Lithuania, pp. 81-88

[6] Wang D., Ternan D., *Image segmentation based on oscillatory correlation*, Neural Computation, **9**, 1997, pp. 805-836.